



Appl. No. 10/696,522  
Amdt. Dated March 13, 2006  
Notice of Allowability mailed December 13, 2005  
Replacement Sheet

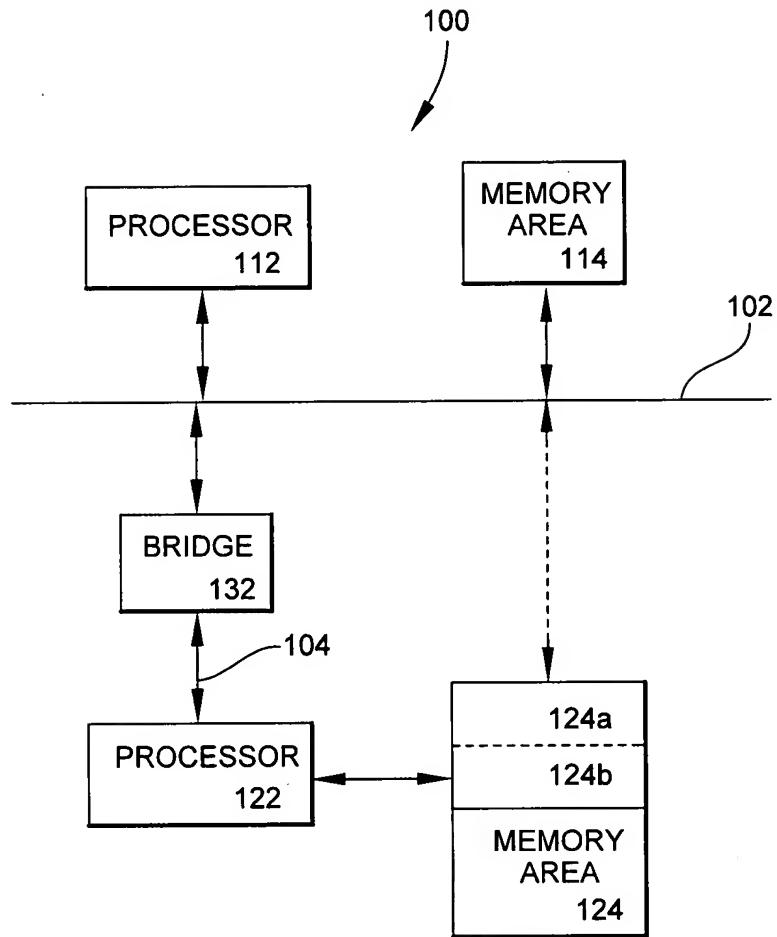
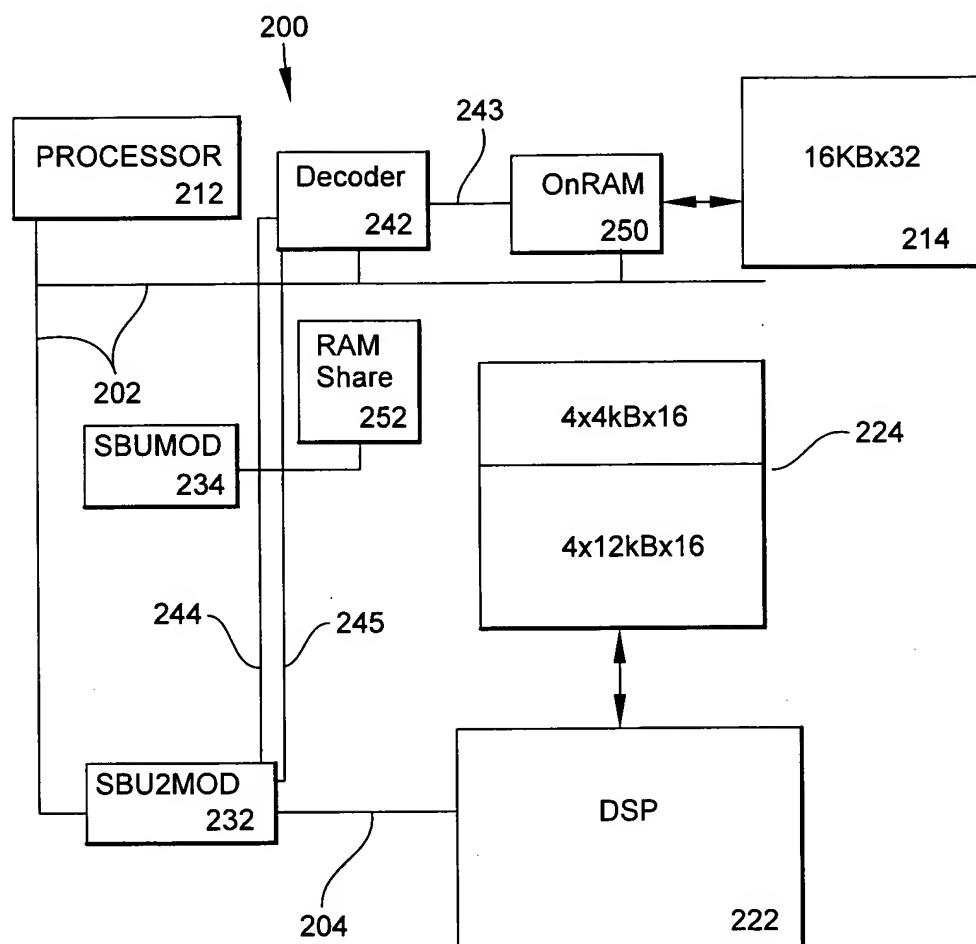


Fig. 1

Fig. 2



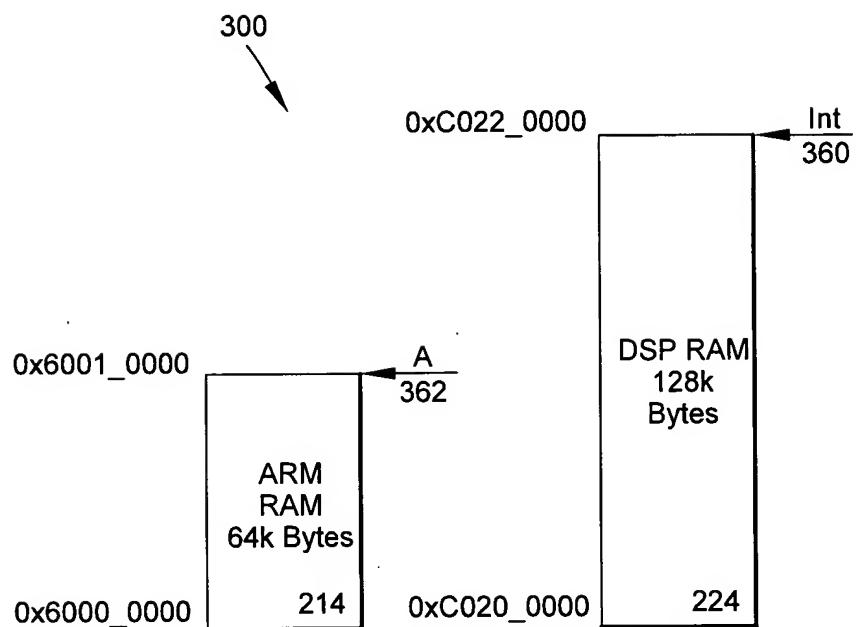
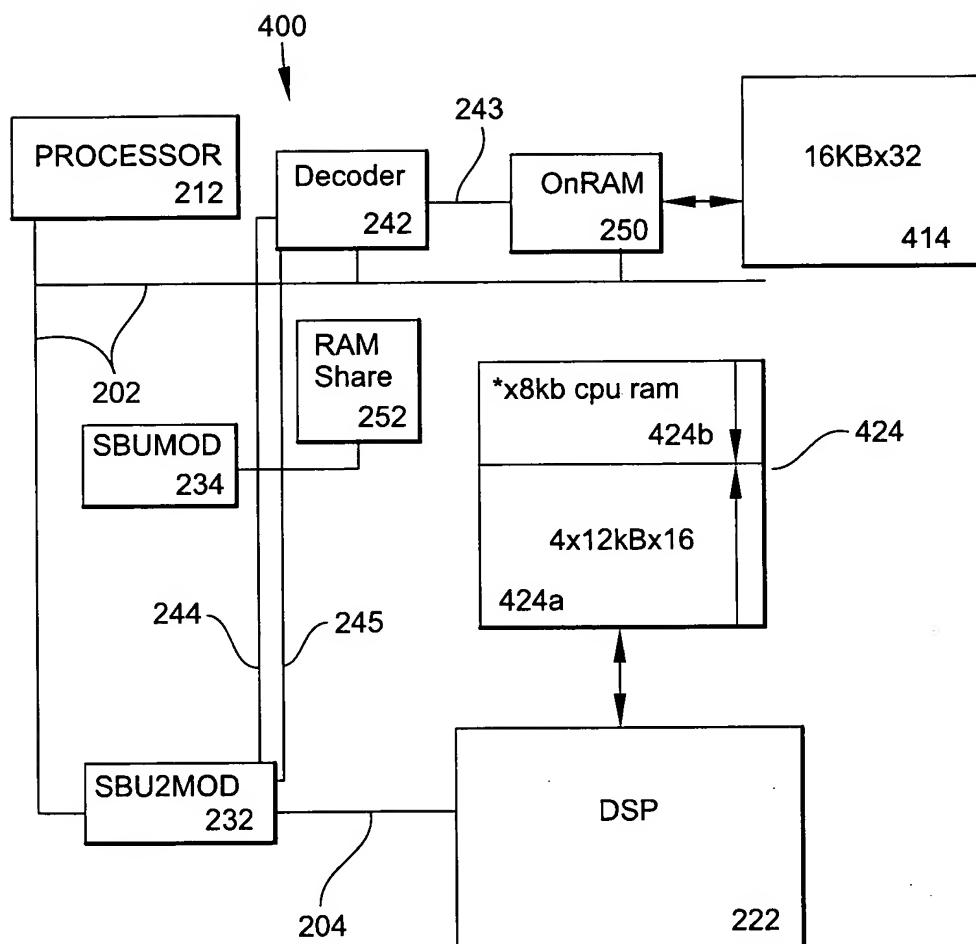


Fig. 3

Fig. 4



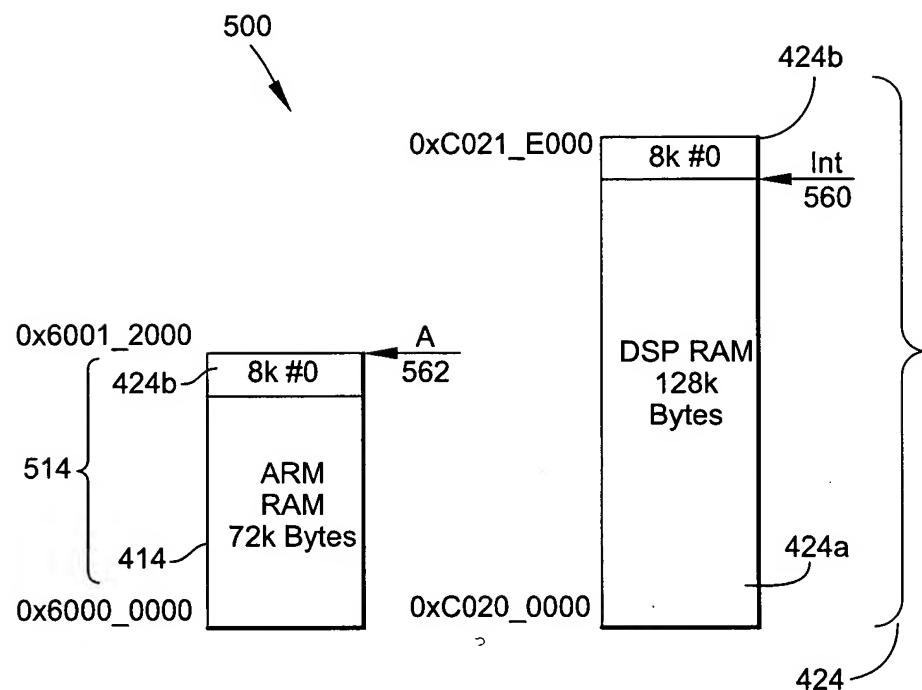


Fig. 5A

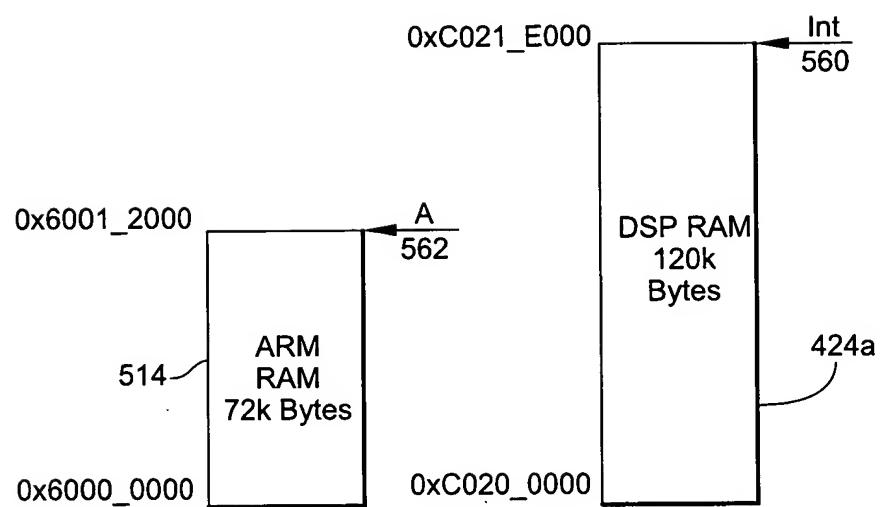


Fig. 5B

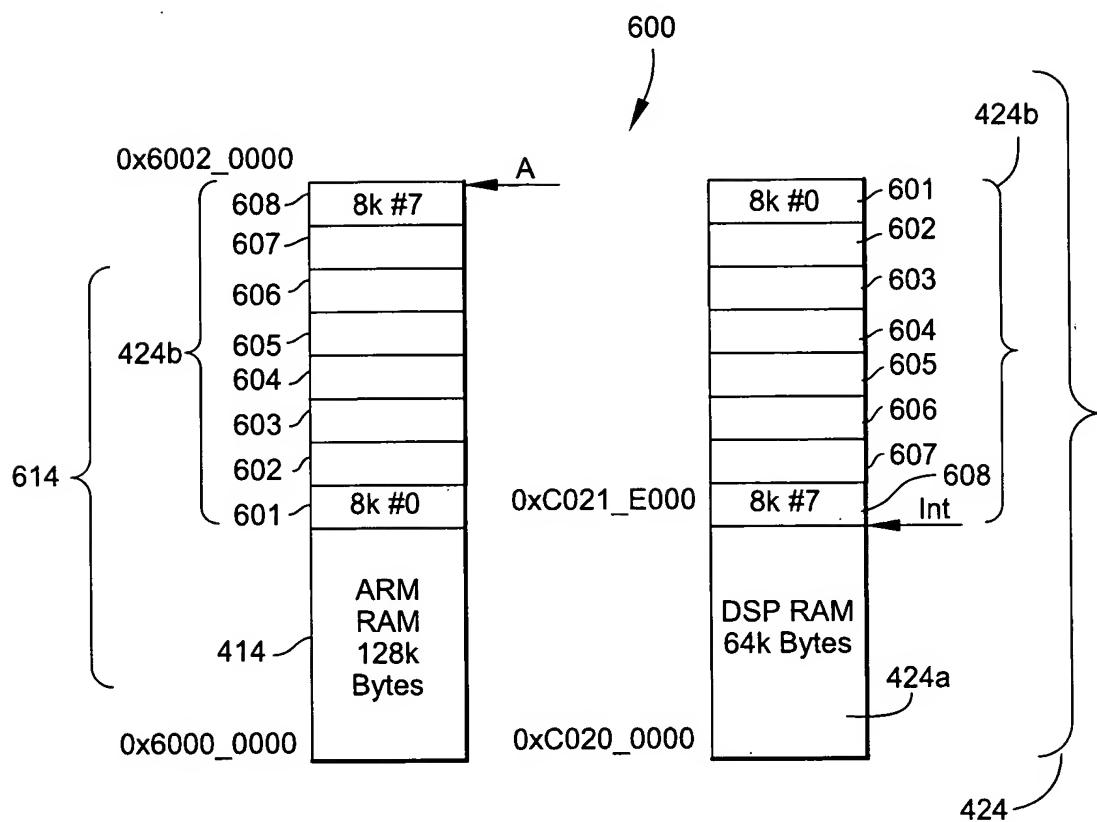


Fig. 6A

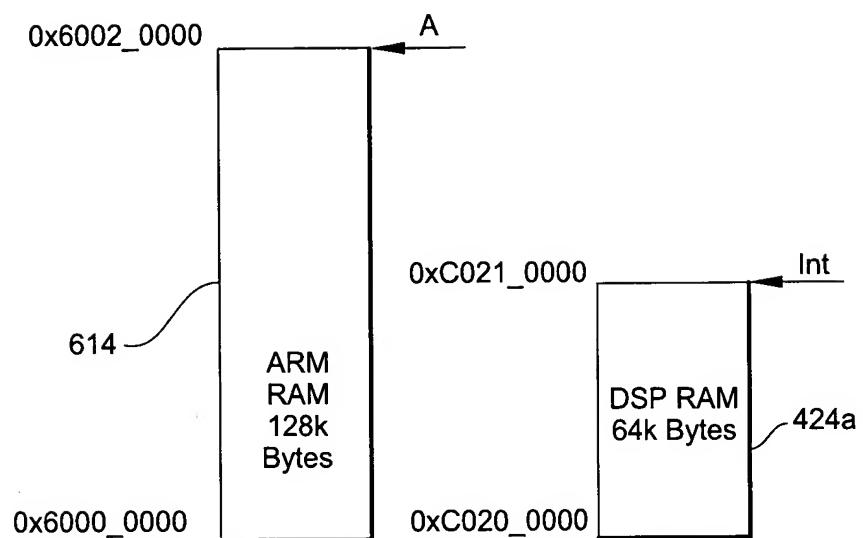


Fig. 6B

Fig. 7

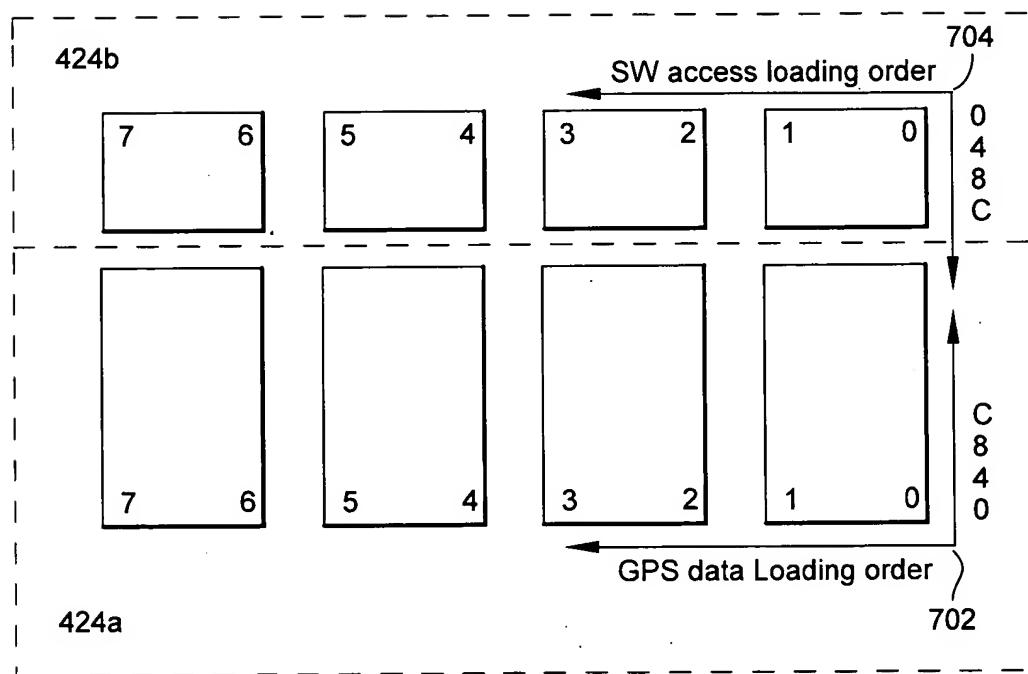
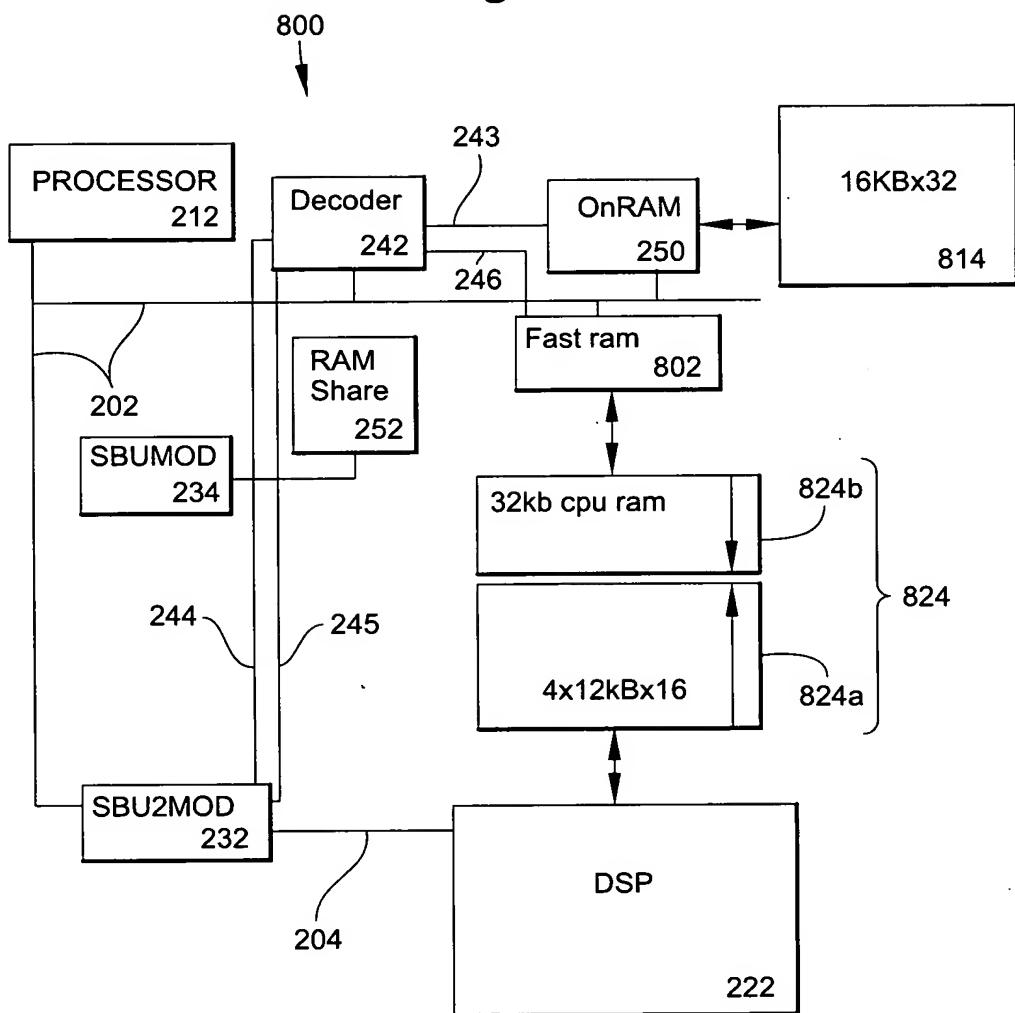


Fig. 8



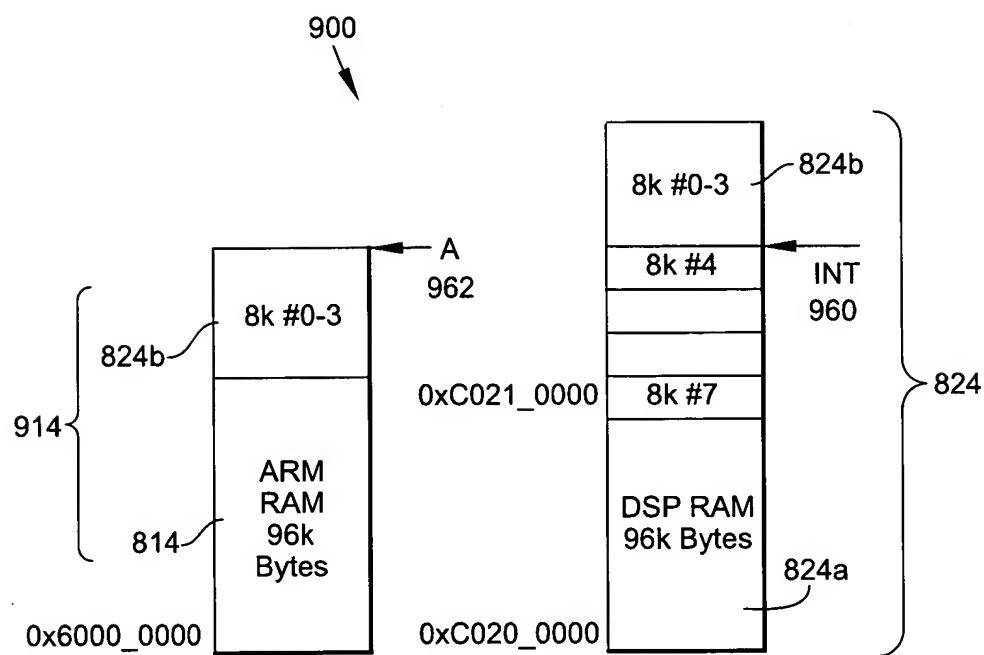


Fig. 9A

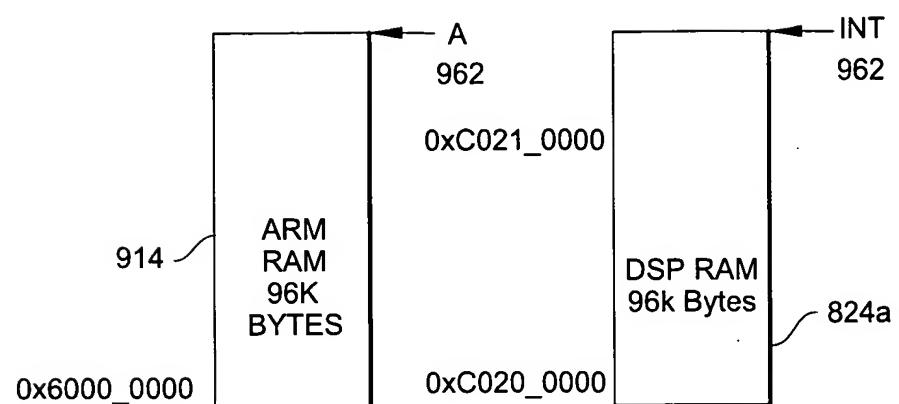
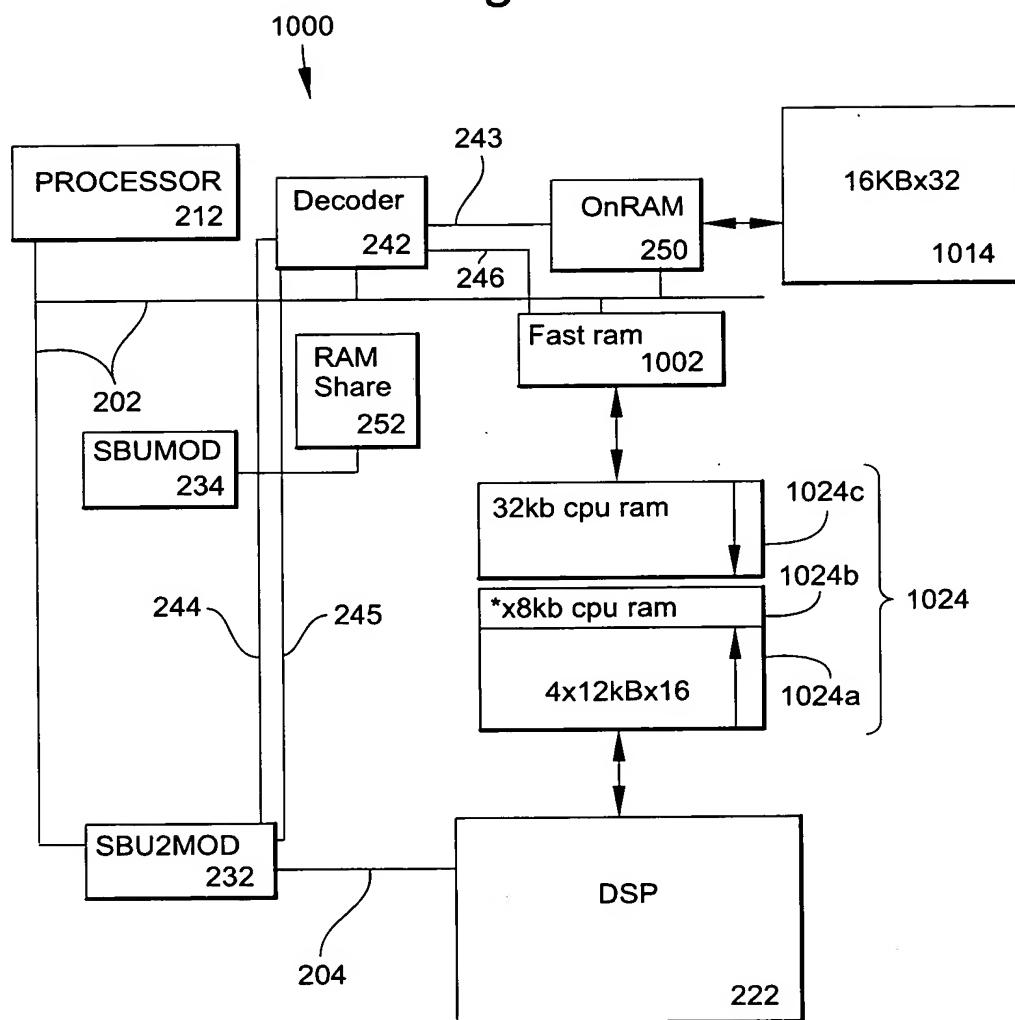


Fig. 9B

Fig. 10



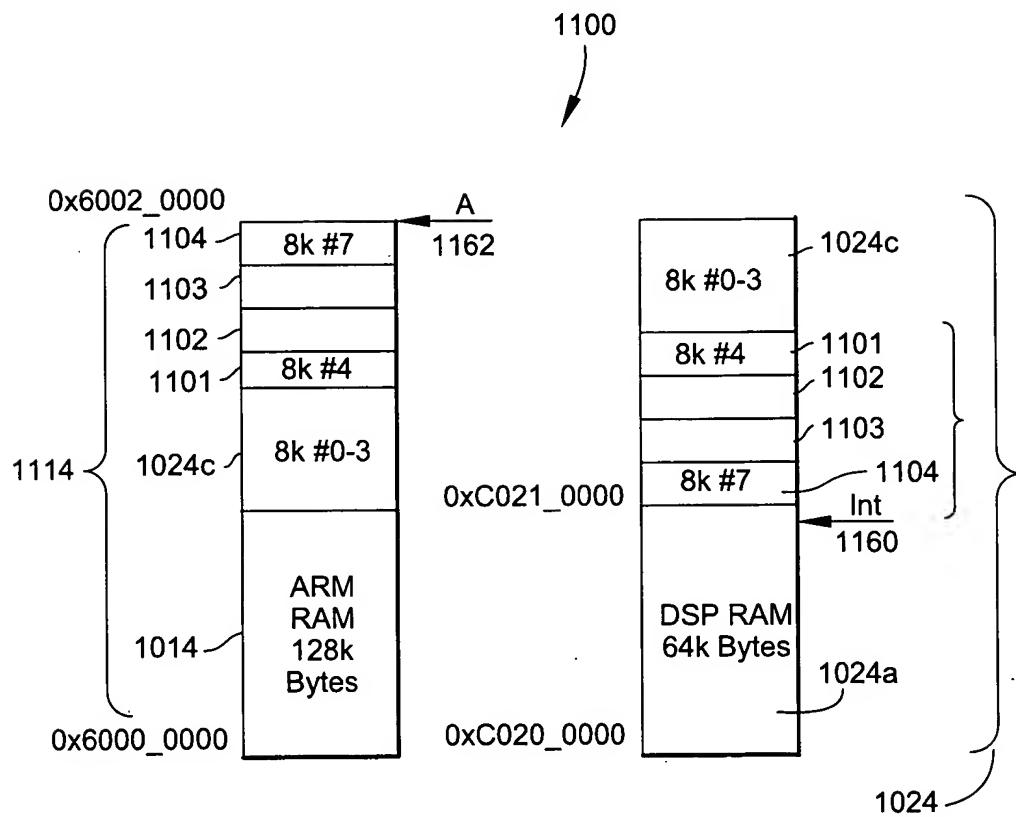


Fig. 11A

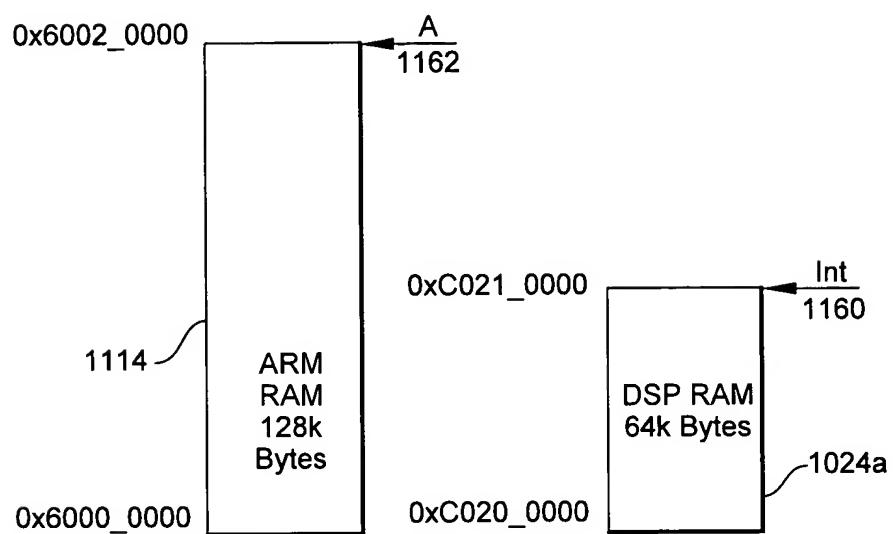


Fig. 11B

Fig. 12

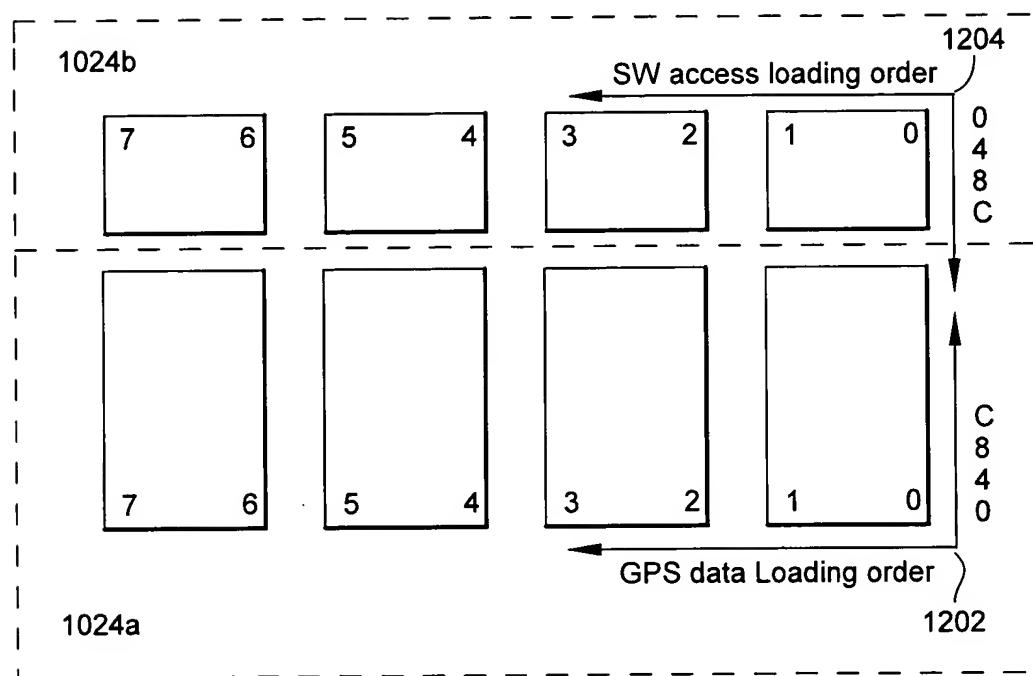
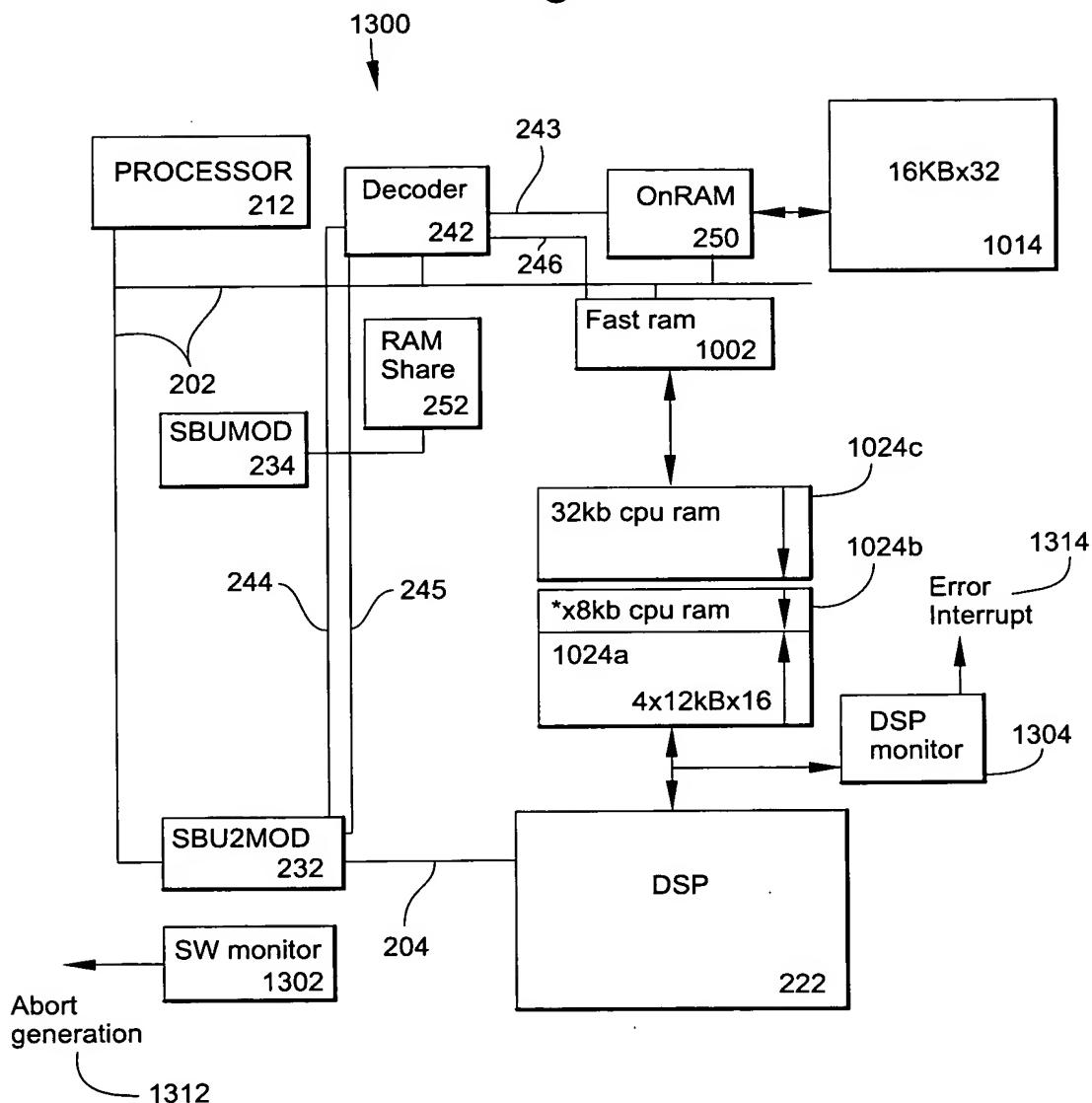


Fig. 13



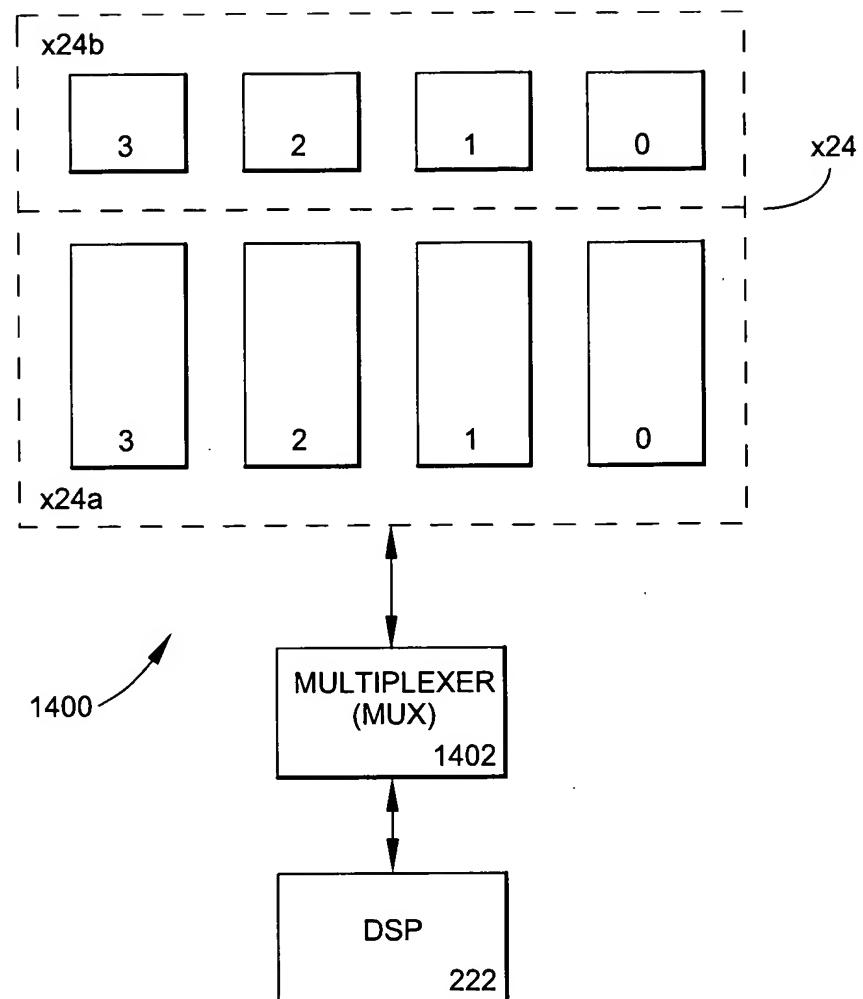


Fig. 14

RAM\_CTL: (address=0xC0000000)

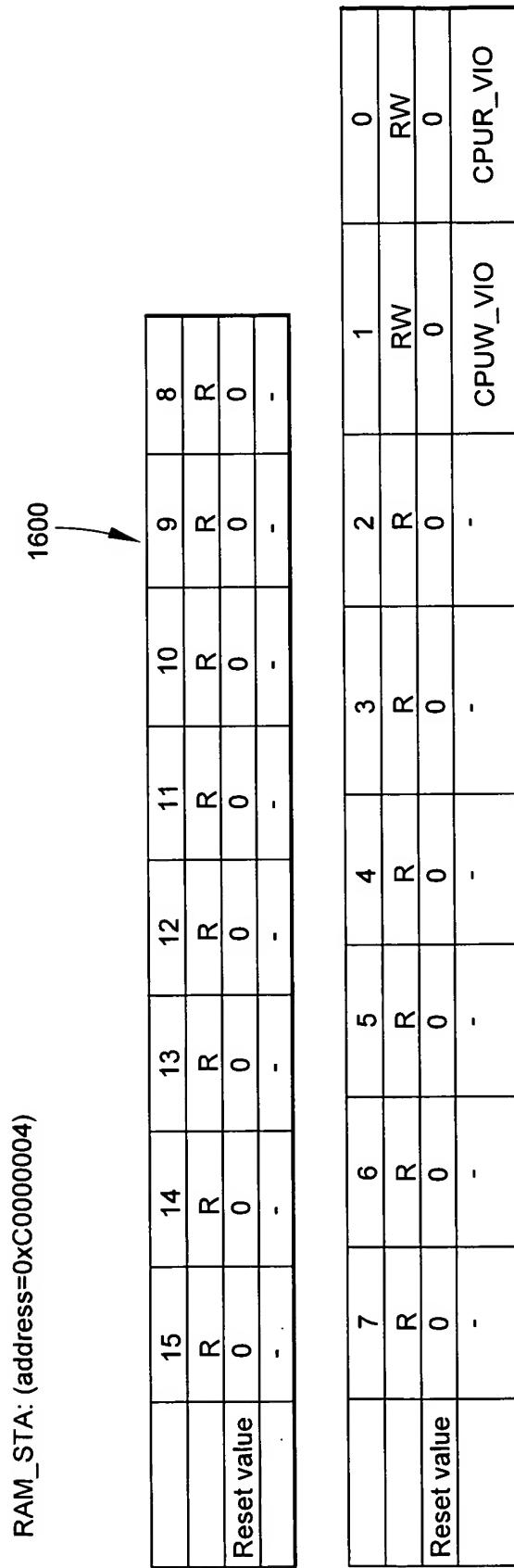
1500



	15	14	13	12	11	10	9	8
	R	R	R	R	R	R	R	RW
Reset value	0	0	0	0	0	0	0	0
	-	-	-	-	-	-	-	-

	7	6	5	4	3	2	1	0
	RW	RW	RW	RW	RW	RW	RW	RW
Reset value	0	0	0	0	0	0	0	0
	SWI_ENB	MAP_BLK[2]	MAP_BLK[1]	MAP_BLK[0]	DSP64K	EN_CPU_WAB	EN_CPU_RAB	MAP_ENB

Fig. 15



RAM\_STA: (address=0xC0000004)

	15	14	13	12	11	10	9	8
	R	R	R	R	R	R	R	R
Reset value	0	0	0	0	0	0	0	0
	-	-	-	-	-	-	-	-

1600

	7	6	5	4	3	2	1	0
	R	R	R	R	R	R	RW	RW
Reset value	0	0	0	0	0	0	0	0
	-	-	-	-	-	-	-	-
							CPUR_VIO	CPUR_VIO

Fig. 16

DSP\_ADDR: (address=0xC0000008)

1700



	15	14	13	12	11	10	9	8
	R	R	R	R	R	R	R	R
Reset value	0	0	0	0	0	0	0	0
DSP_ADD [15]	•	•	•	•	•	•	•	•

	7	6	5	4	3	2	1	0
	R	R	R	R	R	R	R	R
Reset value	0	0	0	0	0	0	0	0
DSP_ADD [0]	•	•	•	•	•	•	•	•

Fig. 17

Fig. 18A

1800  


Number of 8kbyte Blocks Mapped	DSP32K_SWI_ENB	DSP64K_MAP_ENB	MAP_BLK[2:0]	DSP Address Range	CPU Normal Mapped SBU2 Address Range	CPU Soft Mapped SBU2 Address Range	CPU Hard Mapped ASB Address Range
1	0	0	XXX	0x0000_0000-0x0001_FFFF	0xC020_0000-0xC021_FFFF	NA	NA
	1	X	XXX	0x0000_0000-0x0001_7FFF	0xC021_8000-0xC021_FFFF	NA	0x6001_0000-0x6001_7FFF
	0	1	000	0x0000_0000-0x0001_DFFF	0xC021_E000-0xC021_FFFF	0x6001_0000-0x6001_1FFF	NA
2	0	0	XXX	0x0000_0000-0x0001_FFFF	0xC020_0000-0xC021_FFFF	NA	NA
	1	X	XXX	0x0000_0000-0x0001_7FFF	0xC021_8000-0xC021_FFFF	NA	0x6001_0000-0x6001_7FFF
	0	1	001	0x0000_0000-0x0001_BFFF	0xC021_C000-0xC021_FFFF	0x6001_0000-0x6001_3FFF	NA
3	0	0	XXX	0x0000_0000-0x0001_7FFF	0xC020_0000-0xC021_FFFF	NA	NA
	1	X	XXX	0x0000_0000-0x0001_7FFF	0xC021_8000-0xC021_FFFF	NA	0x6001_0000-0x6001_7FFF
	0	1	010	0x0000_0000-0x0001_9FFF	0xC021_A000-0xC021_FFFF	0x6001_0000-0x6001_5FFF	NA
4	0	0	XXX	0x0001_0000-0x0001_FFFF	0xC020_0000-0xC021_FFFF	NA	NA
	1	X	XXX	0x0000_0000-0x0001_7FFF	0xC021_8000-0xC021_FFFF	NA	0x6001_0000-0x6001_7FFF
	0	1	011	0x0000_0000-0x0001_7FFF	0xC021_8000-0xC021_FFFF	0x6001_0000-0x6001_7FFF	NA
5	0	0	XXX	0x0001_0000-0x0001_FFFF	0xC020_0000-0xC021_FFFF	NA	NA
	1	0	XXX	0x0000_0000-0x0001_7FFF	0xC021_8000-0xC021_FFFF	NA	0x6001_0000-0x6001_7FFF
	1	1	100	0x0000_0000-0x0001_5FFF	0xC021_6000-0xC021_FFFF	0x6001_8000-0x6001_9FFF	0x6001_6000-0x6001_7FFF
	0	1	100	0x0000_0000-0x0001_5FFF	0xC021_6000-0xC021_FFFF	0x6001_0000-0x6001_9FFF	NA
6	0	0	XXX	0x0001_0000-0x0001_FFFF	0xC020_0000-0xC021_FFFF	NA	NA
	1	0	XXX	0x0000_0000-0x0001_7FFF	0xC021_8000-0xC021_FFFF	NA	0x6001_0000-0x6001_7FFF
	1	1	101	0x0000_0000-0x0001_3FFF	0xC021_4000-0xC021_FFFF	0x6001_8000-0x6001_BFFF	0x6001_0000-0x6001_7FFF
	1	1	101	0x0000_0000-0x0001_3FFF	0xC021_4000-0xC021_FFFF	0x6001_0000-0x6001_BFFF	NA
7	0	0	XXX	0x0001_0000-0x0001_FFFF	0xC020_0000-0xC021_FFFF	NA	NA

Number of 8kbyte Blocks Mapped	DSP32K_SWI_ENB	DSP64K_MAP_ENB	MAP_BLK[2:0]	DSP Address Range	CPU Normal Mapped SBU2 Address Range	CPU Soft Mapped SBU2 Address Range	CPU Hard Mapped ASB Address Range
	1	0	XXX	0x0000_0000-0x0001_7FFF	0xC021_8000-0xC021_FFFF	NA	0x6001_0000-0x6001_7FFF
	1	1	110	0x0000_0000-0x0001_1FFF	0xC021_2000-0xC021_FFFF	0x6001_8000-0x6001_DFFF	0x6001_0000-0x6001_7FFF
	0	1	110	0x0000_0000-0x0001_1FFF	0xC021_2000-0xC021_FFFF	0x6001_0000-0x6001_DFFF	NA
8	0	0	XXX	0x0001_0000-0x0001_FFFF	0xC020_0000-0xC021_FFFF	NA	NA
	1	0	XXX	0x0000_0000-0x0001_7FFF	0xC021_8000-0xC021_FFFF	NA	0x6001_0000-0x6001_7FFF
	1	1	111	0x0000_0000-0x0000_FFFF	0xC021_0000-0xC021_FFFF	0x6001_8000-0x6001_EFFF	0x6001_0000-0x6001_7FFF
	0	1	111	0x0000_0000-0x0000_FFFF	0xC021_0000-0xC021_FFFF	0x6001_0000-0x6001_FFFF	NA

Fig. 18B

1800